REMARKS

In the outstanding Official Action, claims 1 and 2 were rejected under 35 USC 102(e) as being anticipated by Yoshizaki et al, with claims 1-3 being rejected under 35 USC 102(e) as being anticipated by Coddington and claims 1 and 4-8 being rejected under 35 USC 103(a) as being unpatentable over Applicant's prior art Fig. 1 in view of Yoshizaki, all for the reasons of record. In response, independent claim 1 is herewith amended in order to more particularly and precisely recite the novel and unobvious features of the instant invention, and it is respectfully submitted that claim 1, as herein amended, and the remaining claims depending therefrom are now clearly patentably distinguishable over the cited and applied references for the reasons detailed below.

As herein amended, independent claim 1 now more particularly recites that the control electrode of the first transistor (16) is bias to the supply voltage (6) by a resistor (12) connected in series with two back-to-back connected diode elements (18,19). This arrangement can by clearly seen in Fig. 2, and is described in the associated description of the figure.

In Yoshizaki on the contrary, a substantially different parallel connection of components is shown in the cited Fig. 2.

More particularly, diode-connected elements 8 and 10 are in fact connected in parallel with a resistor 9, rather than in series therewith as in fig. 2 of the instant invention. This is respectfully submitted to be a meaningful distinction, as the parallel-connected circuit of Yoshizaki will operate in a substantially different manner than the series-connected circuit of the instant invention, in particular with respect to transient performance, wherein Yoshizaki provides supply voltage to the control electrode of the transistor immediately via the resistor 9, prior to the diode elements reaching their threshold voltage as required in the instant invention.

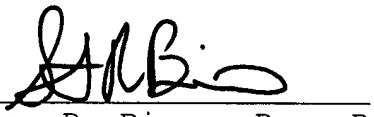
With regard to the Coddington reference, it is respectfully submitted that the cited diode-connected elements (104, 106) in Fig. 2 thereof are not in fact back-to-back connected elements, but rather are elements connected in series between a supply voltage terminal 101 and ground 120.

Finally, it is respectfully submitted that claim 1, as herein amended, and the remaining claims depending therefrom, are clearly patentably distinguishable over Applicant's Fig. 1 in view of Yoshizaki. In relevant part, Applicant's Fig. 1 shows a simple resistive connection between the supply voltage terminal and the gate of the transistor, while Yoshizaki teaches that this resistor is to be connected in parallel with two back-to-back connected

diode elements. Such an arrangement clearly neither shows nor suggests the unique arrangement of Applicant's Fig. 2 wherein the resistor connected to the supply voltage is connected in series with the two-back-two connected diode elements.

In view of the foregoing, it is respectfully submitted that the currently-pending claims, as herein amended, are clearly patentably distinguishable over the cited and applied references. Accordingly, allowance of the instant application is respectfully submitted to be justified at the present time, and favorable consideration is earnestly solicited.

Respectfully submitted,

By 
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